Claims 1-12 are pending in the above-identified application. Claims 1-6, 8-10, and 12 stand rejected. Claims 6, 7 and 11 have been amended.

Claims Objections

Claim 7 stands objected to for various informalities. Regarding the recommendation on page 2 of the January 11, 2002 Office Action (the "Office Action) to change "current controlling circuit" in claim 7 to --gain control unit--, the Applicant respectfully submits that "current controlling circuit" is appropriate. The use of "the current controlling circuit" in claim 7 is appropriate because claim 7 depends from claim 5 which further depends from claim 4 which recites "a current controlling circuit." Applicant has, however, amended claim 7 to incorporate the change which the Examiner suggested for line 6.

Rejection of Claims under 35 U.S.C. § 102

Claims 1-6, 8-10, and 12 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. patent No. 3,991,380 (Pryor). The Applicant respectfully traverses this rejection.

Pryor does not teach or disclose an input buffer including :

> "a first inverting switch connected to a first input voltage and outputting a self bias signal;
>
> a second inverting switch connected to a second input voltage and an output signal; and
>
> a gain control unit having a feedback loop for gain control and responding to the self bias signal and the output signal,"

all as required by independent claim 1. Independent claims 4, 8, and 12 also recite the above-noted circuitry.

Pryor teaches a field effect transistor differential amplifier including two amplifiers which form a feedback circuit (Pryor, col.3, lines 59-65). Page 2 of the Office Action equates output terminal (12) of Figure 2 with the Applicant's claimed self bias signal, however, the Applicant respectfully submits that this is not the case. Figure 2 of Pryor clearly shows that output terminal (12) is not a self bias signal, but rather an output terminal. Further, Pryor makes clear that the output at output terminal (12) matches the output at output terminal (22) (see *e.g.* Pryor, col. 4, line 52 - col. 5 line 26). Thus, Pryor fails to teach a self biasing signal. In the least, then, Pryor fails to a teach a first inverting switch connected to a first input voltage and outputting *a self bias signal*, and a gain control unit having a feedback loop for

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gain control and *responding to the self bias signal and the output signal* (Emphasis added). Accordingly, Applicant respectfully submits that claims 1, 4, 8, and 12 are allowable over Pryor.

With respect to claims 2, 5, and 9, Applicant respectfully submits that page 3 of the Office Action has mis-characterized the connections of transistors P5, P6, N5, and N6 shown in Fig. 2 of Pryor. None of transitors P5, P6, N5 and N6, nor any other parts of Pryor describe a gain control unit as recited in Applicant's claims 2, 5, and 9. Therefore, Applicant respectfully submits that claims 2, 5, and 9 are independently patentable.

Claims 2-3 depend from claim 1 and are allowable for at least this reason. Claims 5-6 depend from claim 4 and are allowable for at least this reason. Claims 9-10 depend from claim 8 and are allowable for at least this reason.

Appreciation is expressed for the indication of allowability of claims 7 and 11. However, Applicant respectfully submits that the amendment as suggested by the Examiner is not required since claims 7 and 11 depend from allowable claims.

In summary, claims 1-12 are pending in the application. This response amends claim 6, 7 and 11 to correct informalities and obvious typographical errors. For the above reasons, Applicant respectfully requests allowance of claims 1-12.

Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned at (408) 453-9200.

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ATTACHMENT A

This response amends claims 6, 7 and 11 as follows. The new material is in bold type face and underlined and the deleted material appears in brackets.

6. (Amended) The input buffer circuit according to claim 5, wherein **the** gain control unit further comprises:

a third PMOS transistor having a source connected to the first node, a gate and a drain connected to the self bias signal;

a third NMOS transistor having a source connected to the second node, a gate and a drain connected to the self bias signal.

7. (Amended) The input buffer circuit of claim 5, wherein the current controlling circuit comprises:

a third PMOS transistor having a source connected to the first node, a drain connected to the gain control unit to supply current and a gate connected to the self bias signal; and

a third NMOS transistor having a source connected to the second node, a drain connected to the gain control unit to sink current and a gate connected to **the** self bias signal.

11. (Amended) The input buffer of claim 8, wherein the swing width control circuit comprises:

an NMOS transistor having a source connected to the **[output signal]gain control unit**, a drain connected to the **[current controlling circuit]gain control unit** and a gate connected to the feedback signal; and

a PMOS transistor having a source connected to the output signal, a drain connected to the**[current controlling circuit]gain control unit** and a gate connected to the feedback signal.

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